REPORT SSD-TR-89-90

The Effect of Elevated Temperature on Latchup and Bit Errors in CMOS Devices

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28 November 1989

Prepared for

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This report was submitted by The Aerospace Corporation, El Segundo, CA 90245, under Contract No. F04701-85-C-0086 with the Space Systems Division, P.O. Box 92960, Los Angeles, CA 90009-2960. It was reviewed and approved for The Aerospace Corporation by H. R. Rugge, Director, Space Sciences Laboratory. Lt Tyron Fisher was the project officer for the Mission-Oriented Investigation and Experimentation (MOIE) Program.

This report has been reviewed by the Public Affairs Office (PAS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited.
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) TR-0086(6940-05)-22	5. MONITORING ORGANIZATION REPORT NUMBER(S) SSD-TR-89-90
6a. NAME OF PERFORMING ORGANIZATION The Aerospace Corporation Laboratory Operations 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION Space Systems Division
6c. ADDRESS (City, State, and ZIP Code) El Segundo, CA 90245-4691	7b. ADDRESS (City, State, and ZIP Code) Los Angeles Air Force Base Los Angeles, CA 90009-2960
8a. NAME OF FUNDING/SPONSORING ORGANIZATION 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER F04701-85-C-0086
8c. ADDRESS (City, State, and ZIP Code)	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT ACCESSION NO.

11. TITLE (Include Security Classification)
The Effect of Elevated Temperature On Latchup and Bit Errors in CMOS Devices

12. PERSONAL AUTHOR(S) Kolasinski, W. A.; Koga, A.; and Schnauss, E. A. (The Aerospace Corporation) Duffey, J. (Hughes Aircraft Co.)

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
	FROM _____ TO _____	1989 November 28	21

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Cyclotron accelerator Heat testing

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Equipment for testing microcircuits at elevated temperatures for Single Event Phenomena (SEP) such as upset (SEU) and latchup (SEL) has been developed, and measurements on several device types have been performed. Very large changes in cross section and threshold Linear Energy Transfer (LET) have been observed over the temperature range of 25°C to 120°C for SEU and SEL.

20 DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	Unclassified
22a NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE (Include Area Code) / 22c. OFFICE SYMBOL

DD FORM 1473, 84 MAR

83 APR edition may be used until exhausted.
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SECURITY CLASSIFICATION OF THIS PAGE
UNCLASSIFIED

PREFACE

We would like to thank Jon Osborn, John Elder, and Bob Walter of The Aerospace Corporation for their generous assistance in the development of the instrumentation, software, and in the collection of data. Our sincere thanks are also due to the members of the LBL 88-in. cyclotron staff, too numerous for individual mention, without whose enthusiastic support and efficient operation of the accelerator, this work would not have been possible.

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I. INTRODUCTION

Tests performed by Cooper et al.[1] on Schottky TTL devices have shown that vulnerability to latchup may increase with temperature. While experience with operational spacecraft leads us to expect that onboard temperatures will range between less than 0°C to nearly 100°C, virtually all testing for vulnerability to Single Event Latchup (SEL) and Single Event Upset (SEU) is currently performed at room temperature. Thus, if the SEU or SEL vulnerability of a mission-critical device depends strongly on temperature, the potential for a catastrophic failure may be missed by ground tests in their present form.

We have attempted to remedy this deficiency in existing test programs by developing instrumentation which enables one to perform latchup and bit-error tests in vacuum, with beams of heavy ions at temperatures in the approximate range of 25-125°C. In developing this hardware, we have tried to maximize the speed of achieving the desired temperature, and the accuracy of maintaining it over long periods of time. Since accelerator time tends to be quite expensive, these features were mandatory for the apparatus to have practical value.

Apart from the practical considerations discussed above, it appeared likely to us that an investigation of Single Event Phenomena (SEP) at elevated temperatures would provide valuable new insights on mechanisms governing these phenomena. The results obtained recently by Stapor et al.[2] on the effect of elevated temperature on SEU induced by protons and alpha-particles tend to support this conjecture.

Following a brief description of the new temperature-control and latchup-detection hardware, we present data on SEL in a commercial CMOS/bulk static RAM and an HCMOS shift register. In the next section we examine SEU data obtained with 16 K RAMs representing CMOS/bulk and NMOS technologies, while in the final section we discuss the implications of the test results and suggest possible avenues of further investigation.

II. INSTRUMENTATION AND TEST METHOD

The tests were carried out at the Lawrence Berkeley Laboratory 88-in. Cyclotron, using 250 MeV krypton ions (LET = 41 MeV-cm^2/mg), 160 MeV argon (LET = 15 MeV-cm^2/mg), 89 MeV neon (LET = 6 MeV-cm^2/mg) and 68 MeV nitrogen-15 (LET = 3 MeV-cm^2/mg). For details of the heavy-ion test techniques, which are by now quite standard, the reader is referred to the technical literature[3,4,5]. The beams of argon, neon, and nitrogen-15 were chosen both for their LET range, and for the special property that when mixed together in, and simultaneously extracted from the Electron Cyclotron Resonance (ECR) ion source, they can be brought individually on target by minor adjustments in the cyclotron frequency. What this means in effect is that any one of three beams with very different LET can be selected by the push of a button.

We now turn to a description of the temperature-test apparatus.

A. TEMPERATURE CONTROLLER

During the initial stages of the temperature tests, all devices on the test board were heated simultaneously while in thermal contact with a copper plate to which a heater had been attached. Because of the large thermal mass of this heating system, long times were required to reach thermal equilibrium, and the maximum temperature that could be achieved with the available power was 55°C. We subsequently developed a new system, where an individual temperature controller in the form of a heater and temperature monitor is mounted in good thermal contact with each test device. A single individual controller is put together using a home-made dual-in-line pin socket, a thermistor, and a small wire-wound power resistor (50 ohms). The test device is plugged into the socket and thermally coupled to the power resistor underneath with high-temperature epoxy or thermal grease. Thermal epoxy is used to attach the thermistor to the top of the delidded chip carrier, next to the recess where the chip is located.

With this arrangement, we were able to reach temperatures in excess of 120°C in less than 5 minutes, starting from room temperature. After a little practice, we could easily maintain the temperature within ± 1°C of the desired value, using a control circuit sensing the thermistor output.

B. AUTOMATIC LATCHUP TESTER

Since the occurrence of latchup is accompanied by a drastic increase in the current drawn by the device, local heating also must take place. It is therefore mandatory that, in the course of controlled temperature testing, the latched condition be detected and cleared before the device has a chance to heat up. Figure 1 shows the circuit we have used to perform the functions of sensing, clearing, and recording latchup in times of a few milliseconds. The current drawn by the test device is sensed across the 1 ohm resistor in the bias-return line. Threshold values of the current can be adjusted by means of the 2 K pot over the range of a few mA to 1 A. Once the current exceeds the preset threshold value, a one-shot is fired after a short adjustable delay of 12-84 ms, the series FET in the Vdd line is turned off, and any capacitors on the Device Under Test (DUT) board are discharged by turning on the FET placed across the DUT power-input lines. The time that the DUT is held off is also adjustable from 8-80 ms. The one-shot pulse is counted in a scaler controlled by the test computer, and after the delay, power is restored to the DUT. Under actual test conditions, the circuit operated very well at rates of several latchup events per second. Even at these rates, devices tested at room temperature showed negligible heating when operated under the latchup-tester control. Under manual operation without the tester, the beam intensity had to be reduced until the SEL rate dropped to no more than one every ten seconds. Still, after several latchups had been cleared by hand, the temperature was observed to approach 40°C. Clearly, the latchup data shown in the next section could not have been obtained without the automatic latchup tester.

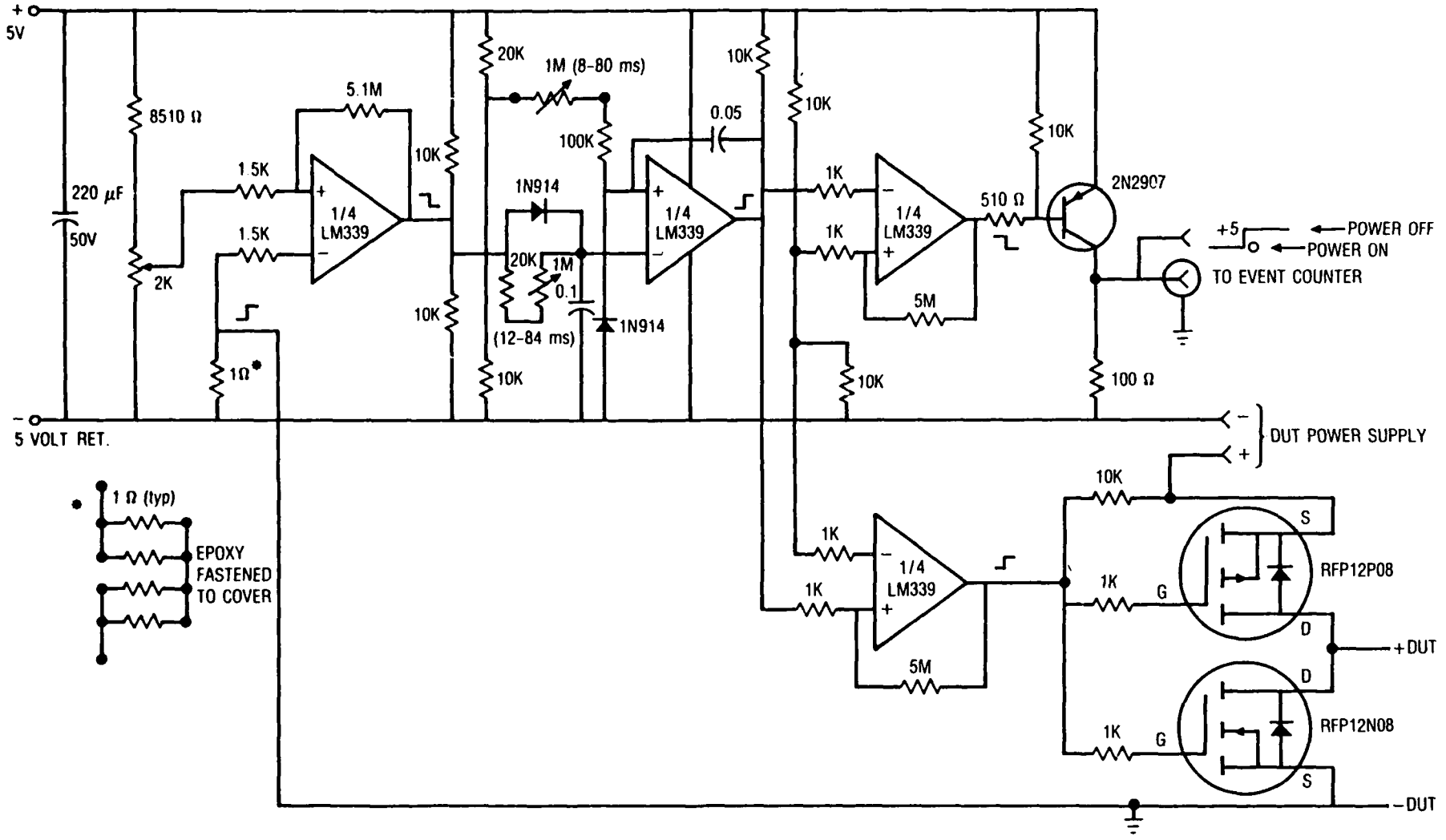

Fig. 1. Schematic Drawing of Latchup Control Circuit

III. RESULTS

In the discussion that follows, "effective LET" is defined as the product of the actual particle LET and the secant of the angle of incidence relative to the chip normal. Unless otherwise pointed out, it will be assumed in the remainder of the discussion that effective LET is the same as the actual LET of a normally incident particle. In the figures that follow, the errors in the data points are typically equal to or smaller than the size of the points themselves.

A. SINGLE EVENT LATCHUP

The latchup data for two samples of one CMOS/ bulk device type (HM6504 4 K × 1 static RAM), representative of several tested, are summarized in Figs. 2 and 3. No latchup was observed at room temperature in case of the serial number (SN) 10 device, for which the 80 and 120°C data appear in Fig. 2. At 80°C we observe a sharp threshold between LET values of 12 and 15 MeV-cm^2/mg, with the SEL cross-section remaining completely flat thereafter at approximately 2×10^{-3} cm^2. At 120°C, the data still show the sharp drop in cross section near an LET of 15 MeV-cm^2/mg, but a new feature, in the form of a shoulder has appeared below the original threshold. Turning to the data for device SN 11, shown in Fig. 3, we see that latchup in this device occurred at room temperature. Apart from this difference, the data at the elevated temperatures agree quite well with those in Fig. 2. Thus, it appears that for this device type and range of LETs used in the tests, the threshold for latchup occurs very close to room temperature.

Turning now to the data for the HCMOS shift register, shown in Fig. 4, we again observe some drastic changes in the SEL cross section over the indicated temperature range. An order of magnitude increase in cross section occurs at high LET values, and threshold LET seems to decrease by 20 to 30 Mev-cm^2/mg. However, the experimental upper limits on cross section at elevated temperature do not rule out a sharp threshold at an LET of 40 MeV-cm^2/mg. At any rate, the observed changes in cross section as a function of LET must translate into large increases in SEL rate at elevated temperatures in space.

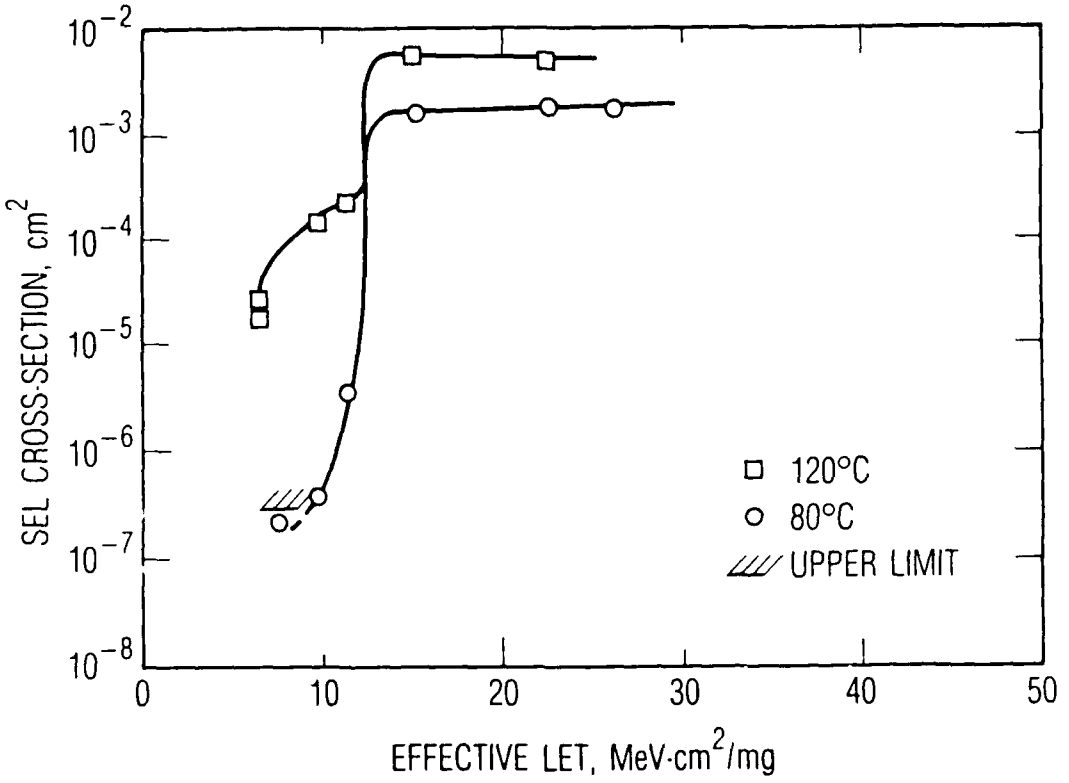

Fig. 2. SEL Results for the HM6504 RAM (SN 10)

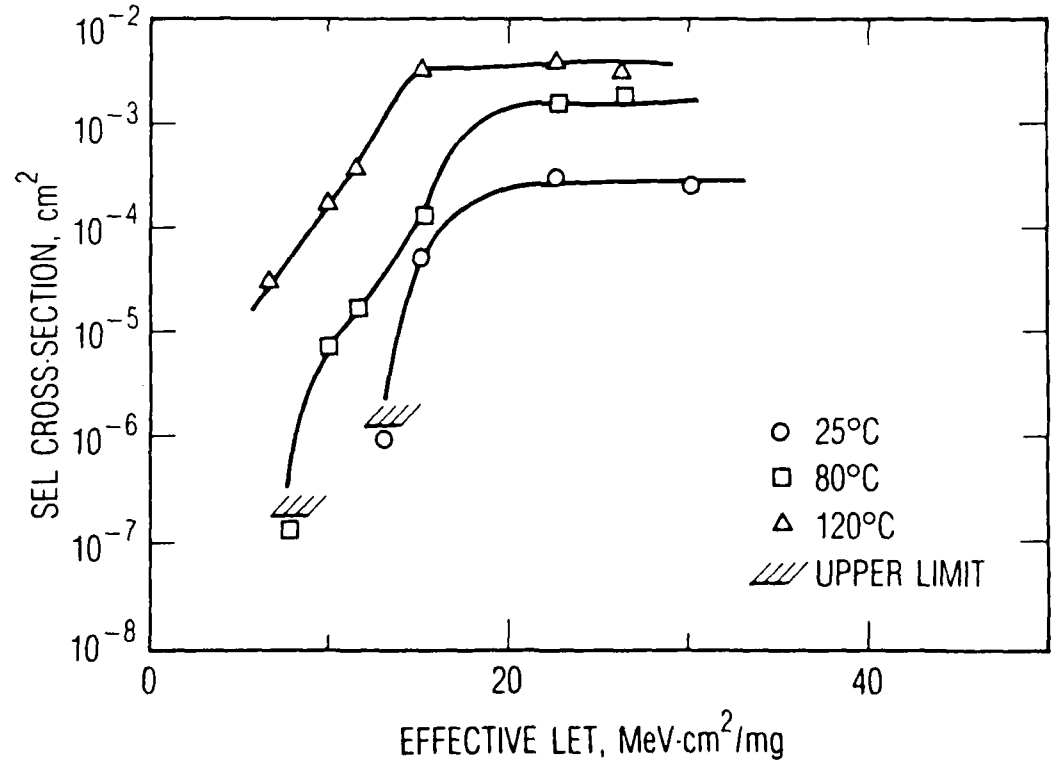

Fig. 3. SEL Results for the HM6504 RAM (SN 11)

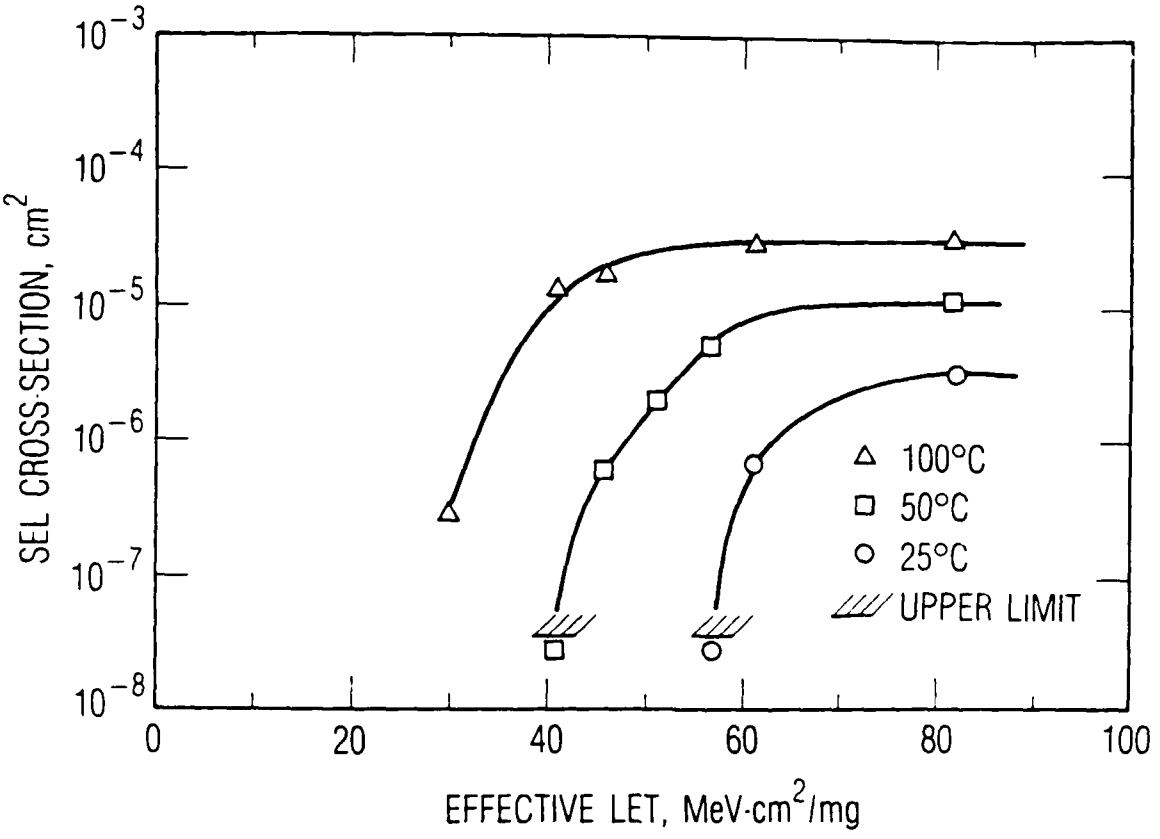

Fig. 4. SEL Results for the 54HC165 Shift Register

B. SINGLE EVENT UPSET

When selecting devices for SEU testing at elevated temperatures, we were guided by the practical consideration of software, hardware, and test-device availability, as well as potential interest in the engineering community. With these considerations in mind, we chose the IDT 2 K × 8 NMOS static RAM (IDT6116) and the Sandia National Laboratory 16 K × 1 CMOS/bulk static RAM (SA3240), with cross-coupling resistors used to suppress SEU. In case of the IDT device, we expected that changes in the biasing resistor values and leakage current with temperature could have a significant effect on the SEU vulnerability. Similarly, the known negative temperature coefficient of resistance of the resistors in the SNL RAMs was expected to lower the threshold LET at high temperature in these RAMs.

We first turn to the IDT6116 data, where Fig. 5 shows the results obtained with argon and nitrogen. These results should be compared with those in Fig. 6, which are for the same device, but with neon substituted for nitrogen. The neon data points in Fig. 6 form a distinct shoulder which becomes more and more pronounced with increasing temperature. In marked contrast, the shoulder is absent in the nitrogen data of Fig. 5 until the 110°C temperature is reached. It appears that in this device type, the concept of effective LET breaks down at LET values below 15 MeV-cm^2/mg.

In testing the SNL RAMs, we obtained data on two devices with 400 K resistors (SN 5551 and 5567) and two with 130 K resistors (SN 5 and 2267). Figure 7 shows the upset cross section, plotted as a function of temperature, for the SN 5551, 400 K device. Onset of errors is observed above 100°C, with a sharp rise in cross section at 120°C taking place. The data were obtained with krypton incident at 60°C (effective LET of 82 MeV-cm^2/mg). No upsets in either of the two 400 K devices were observed with krypton incident normally, at temperatures up to and including 120°C. Figure 8 shows the behavior of the cross section with changing LET for the two devices at 120°C.

Since we did not have ions with sufficiently high LET available to upset the 400 K resistor devices to our satisfaction, we tested some with lower resistor values, and were rewarded with the data shown in Figs. 9 and 10. Features worthy of note here are the apparent saturation of the cross section at values close to 2×10^{-3} cm^2 for high temperature and LET values and low values of bias, as well as the exponential dependence of the cross section on temperature below the saturation region.

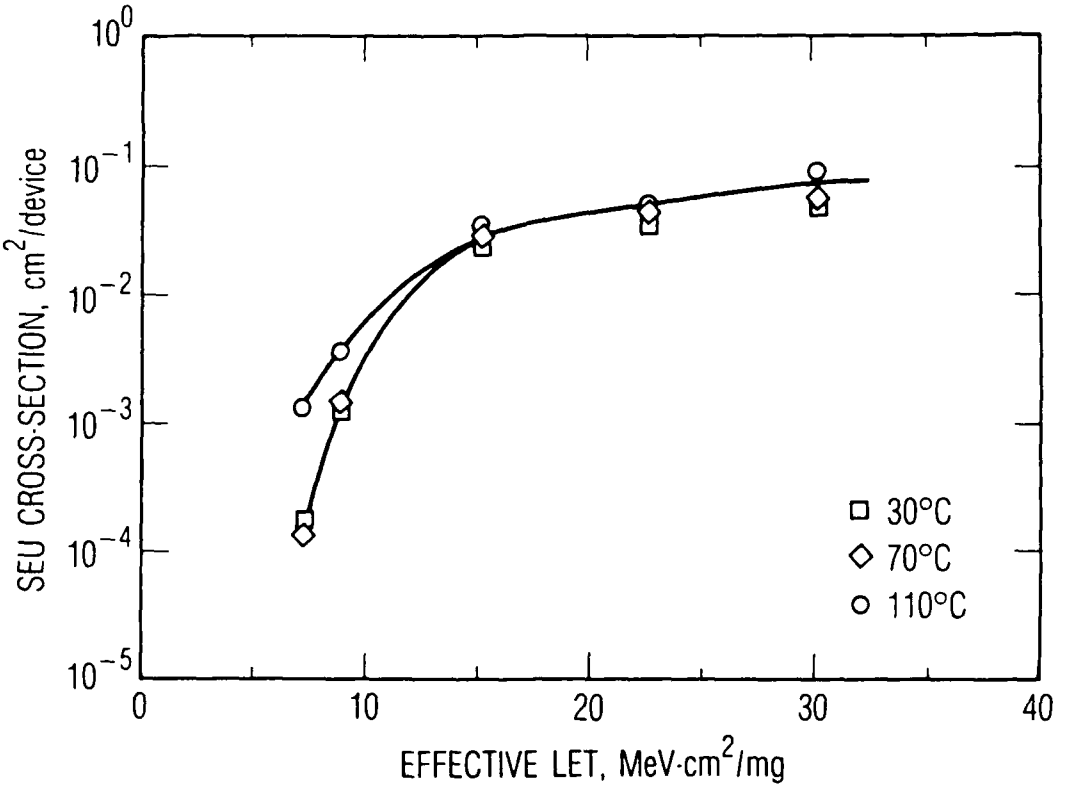

Fig. 5. SEU Results for the IDT6116 NMOS RAM: Argon and Nitrogen Data

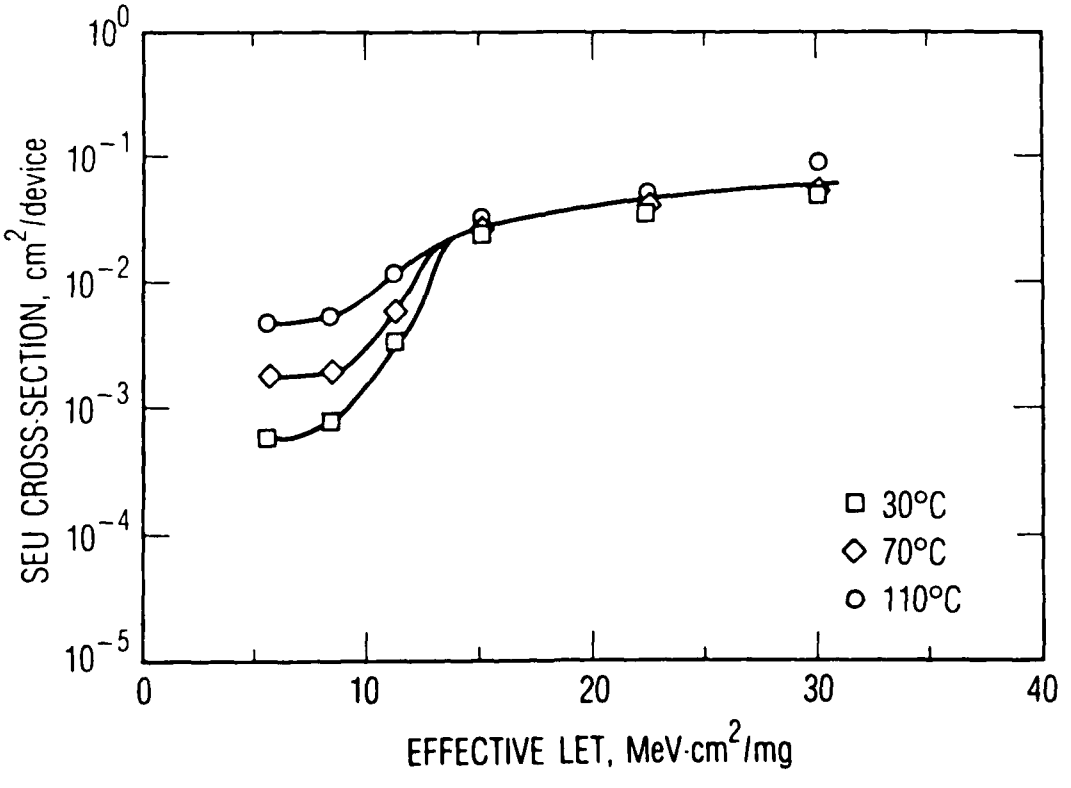

Fig. 6. SEU Results for the IDT6116 NMOS RAM: Argon and Neon Data

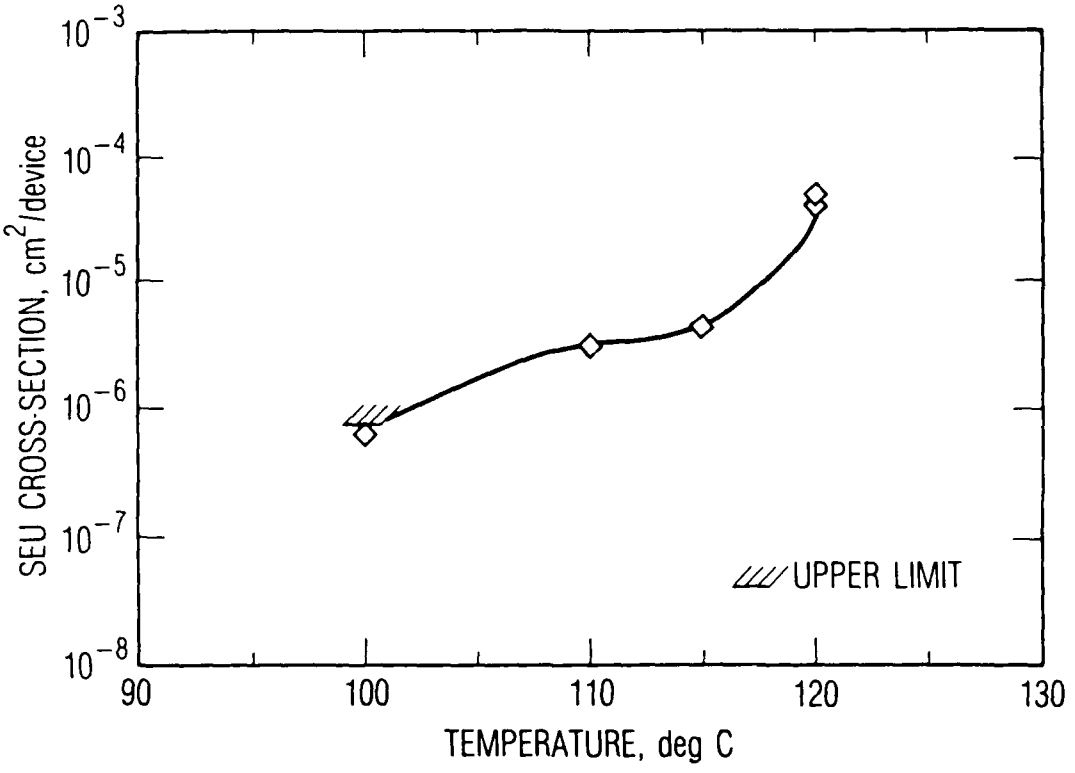

Fig. 7. SEU Results for the SNL SA3240 RAM (400 K Resistor): Cross Section Plotted vs Temperature

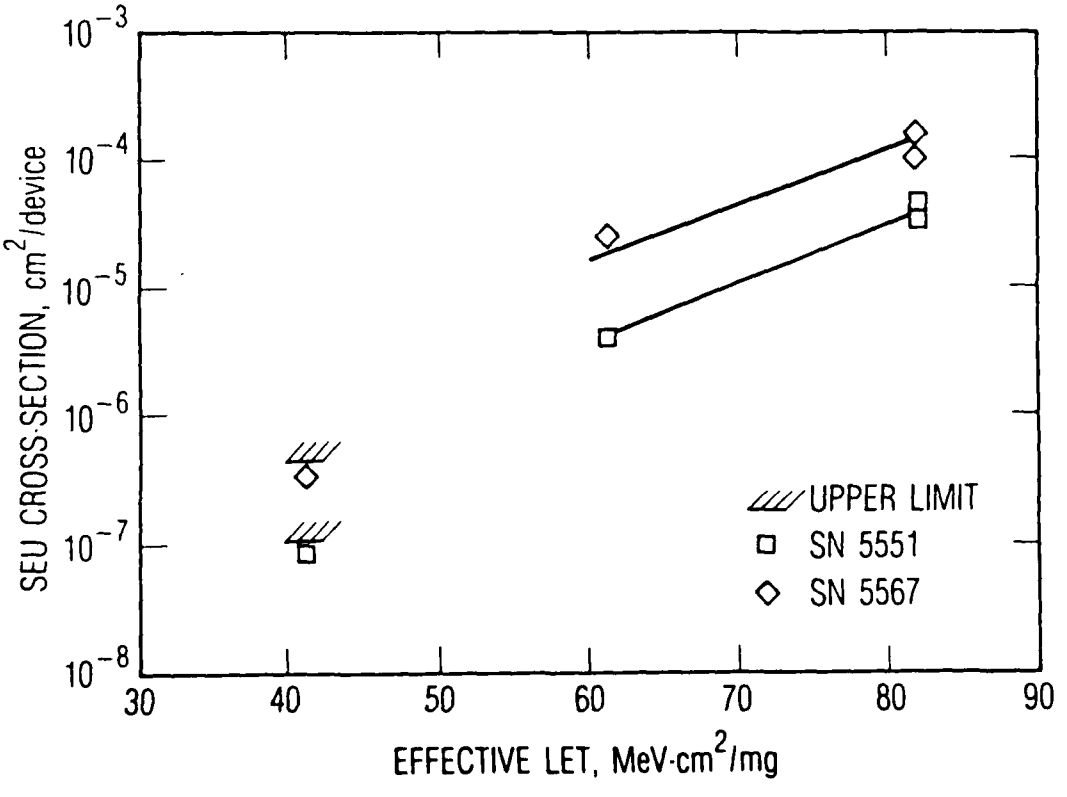

Fig. 8. SEU Results for the SNL SA3240 RAM (400 K Resistor): Cross Section at 120°C vs Effective LET

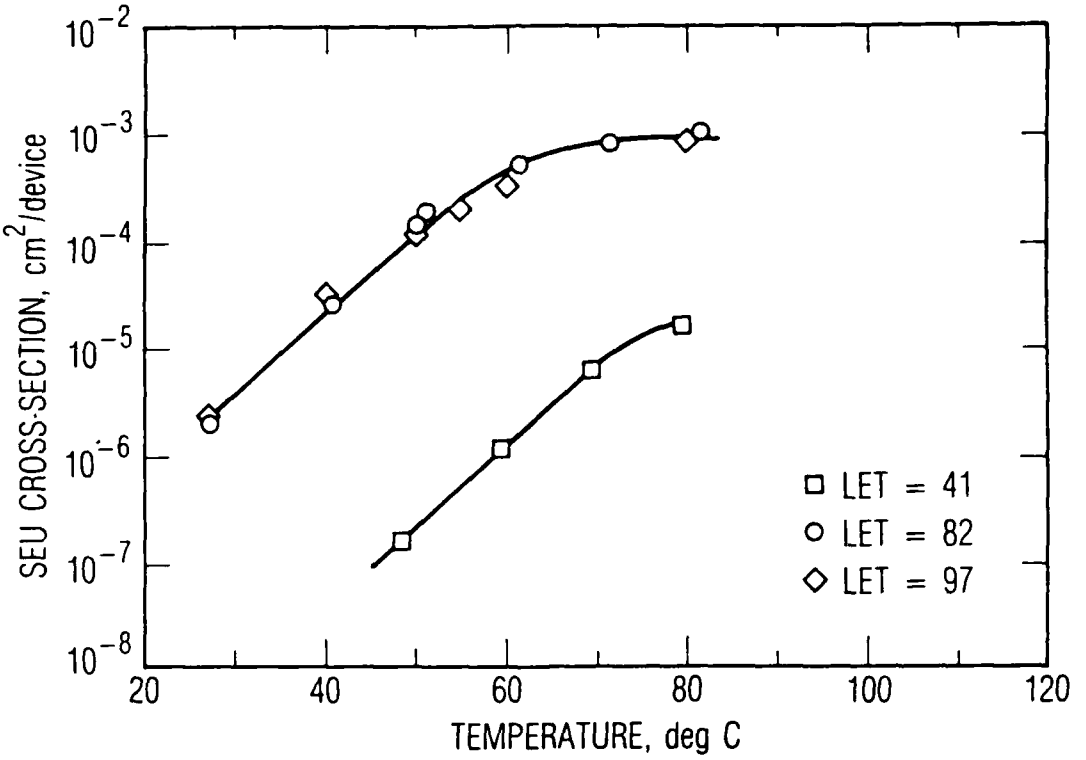

Fig. 9. SEU Results for the SNL SA3240 RAM (130 K Resistor): Cross Section as a Function of Temperature and LET

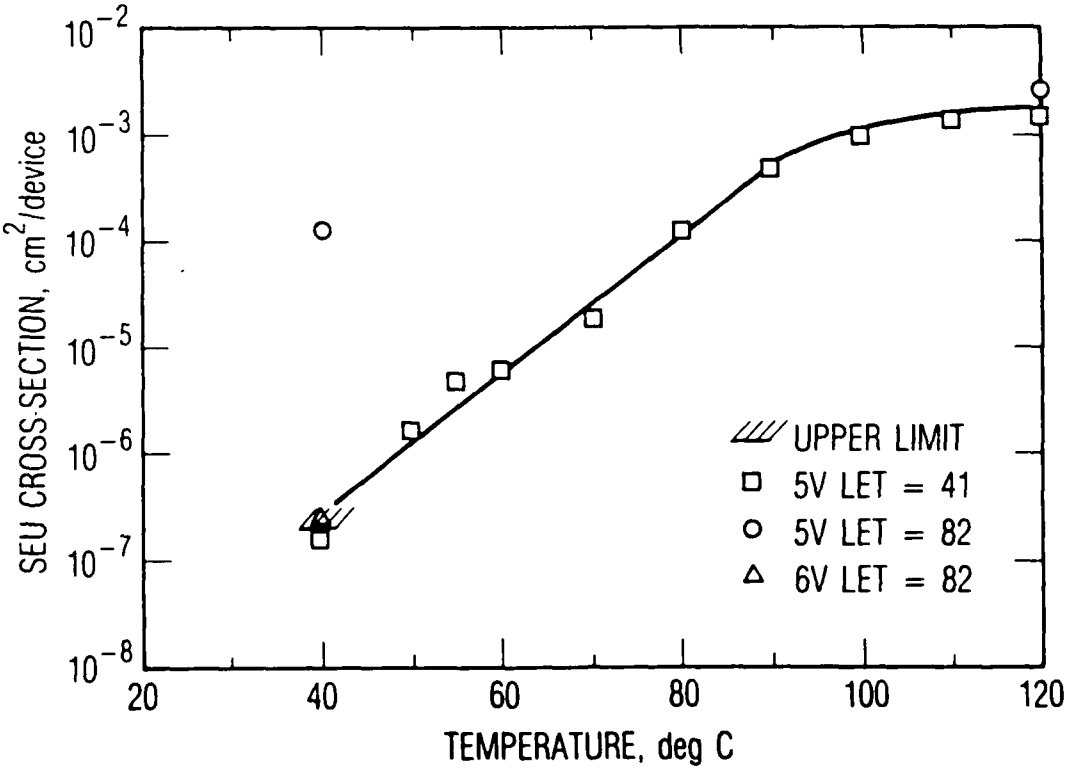

Fig. 10. SEU Results for the SNL SA3240 RAM (130 K Resistor): Cross Section as a Function of Temperature, LET, and Bias

IV. DISCUSSION AND CONCLUSIONS

In looking at the HM6504 RAM latchup data of Figs. 2 and 3, it is difficult to resist making the conjecture that with increasing temperature, new latchup paths with lower threshold LETs enter into the picture, accounting for the appearance of the low LET shoulder. The HM6504 data suggest that once latchup begins to occur along a particular path, the cross-section rises drastically with temperature, while there is relatively little further change in threshold LET. This last observation agrees with the semi-empirical model recently proposed by Shoga and Binder[6], where they point out that the depletion depth (and hence the charge from the incident ion) is very insensitive to temperature. The model, however, does not explain the apparent "quantum" decreases in threshold LET with increasing temperature.

While the 54HC165 data in Fig. 4 show apparent disagreement with the model of Shoga and Binder[6], a very sharp threshold near LET of 40 MeV-cm^2/mg at 100°C cannot be ruled out on the basis of the present results. It is also possible that at cross-section values below the scale range of Fig. 4, the room-temperature data merge with those at elevated temperature. More measurements in the LET range of 30-50 MeV-cm^2/mg are needed to resolve the question whether theory and experiment agree.

An intriguing aspect of the NMOS RAM SEU data is the "normal incidence shoulder" in the cross-section observed with normally incident neon at room temperature and obliquely incident nitrogen at high temperature. All of the ion energies were selected to provide ranges of 30 microns or more, so it is difficult to imagine how range effects could come into play. A plausible explanation is that some sort of strongly angle-dependent funneling effect is taking place. Apart from the just described aspect of the data, the device behavior with temperature does not seem to pose any profound questions. A possible simple explanation for the large increase in cross-section with temperature near threshold LET is that the increased leakage current at high temperature results in a decrease in the device bias, which in turn causes a decrease in critical charge for upset. The simulations performed by Stapor et al.[2], in fact, predict a precipitous drop in critical charge at temperatures above 80°C.

No great surprises are seen in the SNL RAM data. Because of the negative temperature coefficient of the cross-coupling resistors, the critical charge for upset decreases with temperature, resulting in a drastic increase in SEU cross section. This is in complete agreement with the predictions of Diehl et al.[7] We hope that the results will prove of value in validating models used for hardening the devices, and in improvement of future designs.

Several conclusions can be drawn from the work presented above. In the area of latchup and on the practical side, we conclude that for many, if not most devices, room temperature represents a threshold region for latchup. The rather large device-to-device variability in latchup probability observed in the past is explained on that basis. If the above conclusion is correct, the following one is a natural corollary: screening of parts for SEL at elevated temperature should be a firm requirement for critical space-program payloads.

Where support of theory and modeling are concerned, we believe that testing at elevated temperature should be performed on special test structures, where device complexity does not cause the data to be scrambled and difficult, if not impossible, to interpret in terms of model predictions. Furthermore, a microbeam system of the type described by Knudson et al.[8] should provide a large body of extremely useful high-temperature data, and its use should be highly encouraged both on test structures and full-up working devices.

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